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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/712,632	11/13/2000	Alexander L. Minkin	019680-00200US	3726

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EXAMINER	
MONESTIME, MACKLY	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 04/22/2004

13

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/712,632	MINKIN, ALEXANDER L.	
	Examiner	Art Unit	
	Mackly Monestime	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-14 and 33-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-14 and 33-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 10-14 and 33-60 are presented for examination.

Claim Rejections - 35 USC- § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (1) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 10-14, 33-60 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Hook, et al, U.S. Patent 6,353,438.

4. Van Hook et al were cited in the last office action.

5. As per claims 10, 11-14 and 55-60, Van Hook discloses a method of storing a texel in a texel cache (Figures IA, 1B, 1C; Figure 9; Columns 2, lines 9, 20-27, 40-44, 55 through Column 2, line 47; Column 8, lines 20-21; Column 10, lines 8 through Column 11, line 5) comprising: reading *(transferring, requests, texture mapping, texel address information in S and T coordinates, pixels,* Column 10, lines 12, 26-34) a t coordinate of the texel, the t coordinate comprising a. plurality of bits; reading a s coordinate of the texel, the s coordinate comprising a

plurality of bits; and forming an offset *(memory mapping;* Column 11, lines 1-5; 36-47) by concatenating bits of the t coordinate with bits of the s coordinate (.. . the *"resolution" of the pixel is the size of the number value used to describe each pixel. The size of the number value is limited by the number of "bits" in the memory available to describe each pixel ...one hit... two bits.. 32-hit... the number of bits...,* Column 1, lines 45-60; Column 2, lines 20-27; Figures 7 and 8, *tiled caching, address location where the image data (i. e., texels) begins in DRAM... Tile 0 comprises a tile location at S and T coordinates* (SO, To,) *with respect to base address...Each tile comprises a two-dimensional array of texels..., tiles=> texels=> bytes=> bits,* Column 9, lines 16-29, 40-56; Column 10, lines 49- 57;Column 12, lines 5-9; Column 12, lines 57-58, 61-67; *non-contiguous storage locations,* Column 8, line 64 through Column 9, line 1-5; *direct mapped, two-way associative, set associative,* Column 13, lines 12-16, *..the tag index is comprised of the middle hits of the texel,* lines 46-47, *Bits* 0-5, line 51, *middle hits,* lines 60-61, *middle hits,* line 65; Column 14, lines 1-7, *upper bits,* lines 64-66), wherein the texel is associated with a MIP map having a level of detail (Figure 12, Column 7, lines 28-48; Column 15, lines 58-59; Column 16, lines 38 through Column 17, line 17) comprising a plurality of bits, further comprising forming an index signal (Column 7, lines 20-34; 42-47, *an index assigned to a specific cache line . .... tag information identifies the tile..)* by concatenating middle order bits of the s coordinate, middle level bits of the t coordinate, and at least one bit of the level of detail (Figures 7-9, 11-12, *resolution, trilinear MIP-mapping,* see *pixel valves* above; Column 4, lines 8-47).

6. AS per claims 11 and 58, Van Hook et al disclosed texture identification (see above, Column 7, line 27, *tag information identifies)* at least one bit of the texture identification (see *hits* above).

7. As per claims 12 and 59, Van Hook et al disclosed r coordinate (see above; [Examiner interprets that the r coordinate is used in texturing applications using a r, s and t coordinate system, as Van Hook discloses: 3D *trilinear mipmapping...ftltering, RCB, depth cueing,* Column 2, lines 35-54; Column 15, lines 8-1 1; 34-35) at least one bit of the r coordinate (see *hits* above);

8. As per claim 13 and 60, Van Hook et al disclosed: a main memory address (Figures 7-9, see above, DRAM, Column 7, lines 23-25), at least one bit of the main memory address (see bits above).

9. As per claims 14 and 56, Van Hook et al disclosed: an integrated circuit (Figures 10A, element 1030; 1013, Column 17, lines 50-54) comprising: a texture cache subsystem for storing a texel (Figure 9, element 901); a cache address generator subsystem configured to provide an index and offset to the texture cache subsystem (903); and a graphics pipeline subsystem configured to provide an s coordinate, a t coordinate, and a memory address to the cache address generator subsystem (904), and further configured to receive the texel from the texture cache subsystem, wherein the index comprises bits of the s and t coordinates and at least on bit selected from the group consisting of level of detail, a texture id, a memory address, and an r coordinate (see above); furthermore, Van Hook et al disclosed a FIFO (Column 6, line 35) coupled to receive packets of data (Figures l0A and 10B, element 1025, Column 19, lines 1-5, see above), from the texture cache manager, where the FIFO stores the packets of data for a plurality of clock cycles (Column 15, lines 1-2, 13-14, 15-25).

10. As per claim 33, representative of claims 38, 43, 48, Van Hook discloses the method of claim 10, wherein the forming an offset by concatenating bits of the t coordinate with bits of the s coordinate is done by concatenating the lower bits of the t coordinate with the lower order bits of the s coordinate (Column 11, lines 1-4; Column 13, lines 36-62).

11. As per claim 34, representative of claims 39, 44, 49, 53, Van Hook disclosed the method of claim 33 further comprising storing the texel in a texel cache comprising a plurality of cache lines, wherein each cache line comprises a plurality of storage elements (see above; Column 7, line 9-1 1).

12. As per claim 35, representative of claims 40, 4:5, 50, 54,Van Hook discloses the method of claim 34 further comprising storing the texel in a storage element identified by the offset (see above; Column 8, line 64 through Column 9, line 5), the storage element in a cache line, the cache line identified by the index (see above; Column 7, lines 1-12, 20-50).

13. As per claim 36, representative of claims 41, 46, 51, Van Hook discloses the method of claim 35 further comprising retrieving the texel from a main memory, wherein the texel has an address in main memory (Column 1, line 40 through Column 2, lines 67).

14. As per claim 37, representative of claims 42, 47, 52, Van Hook discloses the method of claim 36 further comprising forming a tag by concatenating the high order bits of the s coordinate and high order bits of the t coordinate, adding tile address in main memory, and storing the tag in a look-up table (Figure'), Column 7, line 21).

15. As per claim 55, Van Hook discloses the circuit of claim 54, further comprising a memory controller coupled to the texture cache subsystem, the memory controller configured to

receive and provide texels from and to an external memory (Figures 10A and 10B, elements 1030A, 1015, 1032, 103013, 1014, Column 18, lines 11-24).

Response to Arguments

16. Applicant's arguments filed on February 8, 2004 have been fully considered but they are not persuasive. As per claim 10, applicant argued that Van Hook et al did not disclose using a portion of a level of detail as part of index signal and a tag signal. However, Van Hook et al did disclosed the level of detail may be specified as a portion of the tag information (col. 7, lines 38-39); wherein the tag information for a given texel contains addressing information regarding its location in DRAM; moreover, a portion of the texel information is utilized as an index assigned to a specific cache line; and another portion of the tag information identifies the tile currently stored in cache (col. 7, lines 23-28) and a portion of the S bits and a portion of the T bits are utilized as the index and tile information, and wherein the upper S bits and upper T bits are utilized to identify the tag currently in cache at the cache line specified by the tag index. Therefore, Van Hook et al did disclose such limitations.

17. As per claim 11, applicant argued that Van Hook et al did not disclose middle order bits of s and t coordinates and at least one bit of texture identification. However, Van Hook et al did teach a two-dimensional texture or pattern image that is mapped onto a two dimensional surface; wherein a two-dimensional surface, X and Y coordinates may be sufficient for defining a mapping function between pixels forming the surface and texels forming the texture image (col. 1, lines 35-39); a brick pattern stored as a texture image referenced by s and t coordinates (col. 3, lines 8-11); Van Hook et al further disclosed to exploit the 2D nature of texel information, a

portion of the S bits and a portion of the T bits are utilized as the index and tile information. For example, in one embodiment, the middle S bits and middle T bits are utilized as the tag index (col. 7, lines 28-34) and an address identifies each texel with the most significant bits identifying the particular tile that the texel is located within (col. 12, lines 65-67). Applicant further argued that at least one bit of the texture identification as part of an index signal reduces trashing in a texture cache. In this presence instance, applicant is arguing a feature of the invention not specifically stated in the claim language, which is improper. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. ***In re Self***, 213 USPQ 1, 5 (CCPA 1982); ***In re Priest***, 199 USPQ 11, 15 (CCPA 1978). Therefore, Van Hook et al did disclose such limitations.

18. As per claim 12, applicant argued that Van Hook et al did not disclose at least one bit of the r coordinate. However, Van Hook et al disclosed a three dimensional surface, a perspective coordinate or other depth cueing can be used to indicate distance from the viewing plane (using r, s, t as coordinates of the 3D texture image; col. 2, lines 39-54). Applicant further argued that at least one bit of the r coordinate as part of an index signal reduces trashing in a texture cache. In this presence instance, applicant is arguing a feature of the invention not specifically stated in the claim language, which is improper. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. ***In re Self***, 213 USPQ 1, 5 (CCPA 1982); ***In re Priest***, 199 USPQ 11, 15 (CCPA 1978). Therefore, Van Hook et al did disclose such limitations.

19. As per claim 13, applicant argued that Van Hook et al did not disclose at least one bit of the main memory. However, Van Hook et al disclosed a cache tag identifies the DRAM location

that a tile or texel currently in cache originated from; and wherein the tag identifies the tile that the texel location in the DRAM (col. 13, lines 36-63). Applicant further argued that at least one bit of the r coordinate as part of an index signal reduces trashing in a texture cache. In this presence instance, applicant is arguing a feature of the invention not specifically stated in the claim language, which is improper. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. ***In re Self***, 213 USPQ 1, 5 (CCPA 1982); ***In re Priest***, 199 USPQ 11, 15 (CCPA 1978). Therefore, Van Hook et al did disclose such limitations.

20. As per claims 14 and 56, the limitations are similar to claims 10, 11-13, and so the responses presented above apply with equal force to claims 14 and 56.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mackly Monestime whose telephone number is (703) 305-3855. The examiner can normally be reached on Monday to Thursday from 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bella Matthew, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patent and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Mackly Monestime

Patent Examiner

April 13, 2004

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600